

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
8 July 2004 (08.07.2004)

PCT

(10) International Publication Number
WO 2004/057487 A3

(51) International Patent Classification⁷: **G06F 15/80**

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(21) International Application Number:
PCT/GB2003/005451

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(22) International Filing Date:
12 December 2003 (12.12.2003)

(81) Designated State (*national*): US.

(25) Filing Language: English

(84) Designated States (*regional*): European patent (AT, BE,
BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU,
IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR).

(26) Publication Language: English

(30) Priority Data:
0229788.5 20 December 2002 (20.12.2002) GB

Published:

- with international search report
- before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments

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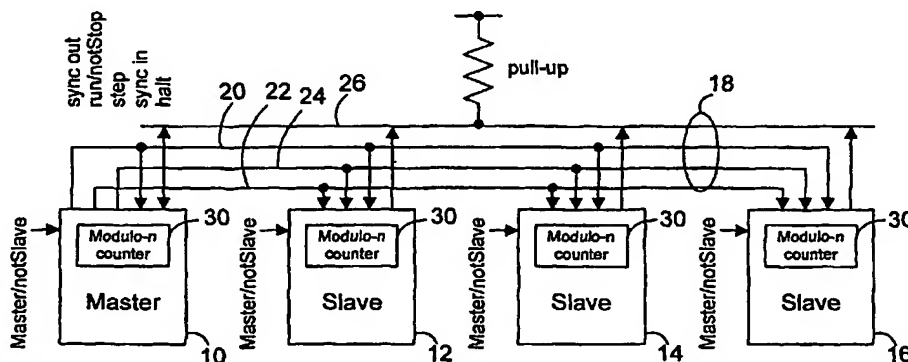
(88) Date of publication of the international search report:
10 February 2005

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*For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*

(54) Title: ARRAY SYNCHRONISATION



(57) Abstract: A method is disclosed for achieving synchronization in an array of semi-synchronous devices. A processor array has an array of processor elements, wherein each of said processor elements comprises a cycle counter, and a master processor element is able to transmit control command signals to each of the other processor elements. Each processor element is such that, on receipt of a control command signal, it acts on that signal only when its cycle counter reaches a predetermined value, and the master processor element is such that it transmits control command signals only when its cycle counter takes a value which is within a predetermined range, or "safe window". By appropriate setting of the "safe window", it can be guaranteed that, when the master processor element transmits a control command signal to each of the other processor elements, those command control signals are acted upon at corresponding times within the other processor elements.

INTERNATIONAL SEARCH REPORT

ational Application No

/GB 03/05451

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F15/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GREENSTREET M R: "Implementing a STARI chip" COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS, 1995. ICCD '95. PROCEEDINGS., 1995 IEEE INTERNATIONAL CONFERENCE ON AUSTIN, TX, USA 2-4 OCT. 1995, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 2 October 1995 (1995-10-02), pages 38-43, XP010197289 ISBN: 0-8186-7165-3 page 38, left-hand column - page 39, right-hand column; figure 1	1-10
A	US 6 055 285 A (ALSTON JERALD) 25 April 2000 (2000-04-25) columns 5-8 ----- -/--	1



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

2 December 2004

Date of mailing of the international search report

10/12/2004

Name and mailing address of the ISA

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INTERNATIONAL SEARCH REPORT

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/GB 03/05451

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>WO 02/50700 A (CLAYDON ANTHONY PETER JOHN ; PICOCHIP DESIGNS LTD (GB)) 27 June 2002 (2002-06-27) page 11 pages 17-19; figure 1 -----</p>	1

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tional Application No

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			AU 9576801 A	01-07-2002
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			JP 2004525440 T	19-08-2004